NCSR Demokritos' Contribution to the Public Consultation on the Chips Act 2.0

General position

NCSR Demokritos welcomes the European Commission's proposal for the Chips Act 2.0 and supports its objectives of strengthening Europe's semiconductor ecosystem, reducing strategic dependencies, accelerating the industrial deployment of European research and innovation, and improving the resilience and security of semiconductor supply chains. The proposal appropriately recognises the importance of advanced manufacturing equipment and processing, mainstream and specialty semiconductor technologies, integrated photonics, quantum chips, pilot lines, design capacities and competence centres. It also introduces valuable instruments, including Grand Challenges, European Semiconductor Technology Initiatives and Strategic Projects. NCSR Demokritos nevertheless considers that several provisions could be further strengthened to:

- better mobilise Europe's distributed research and technology capabilities;
- support the development and industrialisation of advanced materials, new manufacturing processes and specialty semiconductor technologies;
- maintain a balanced portfolio of low- and medium-TRL research capable of generating new knowledge, process expertise and specialised talent for Europe's semiconductor industry;
- ensure the technological renewal of competence centres and research infrastructures;
- establish transparent pathways from research to pilot-scale validation and industrial deployment;
- reinforce the participation of independent scientific and technical expertise in European semiconductor governance;
- provide appropriate financial support for recognised Strategic Projects and European Semiconductor Technology Initiatives; and
- promote the coordinated development and validation of AI-driven methods for semiconductor materials, manufacturing processes, metrology and characterisation;
- strengthen circularity, component reuse and sustainable semiconductor manufacturing.

The following amendments are therefore proposed.

1. Advanced materials as a foundation for next-generation semiconductor and AI hardware

Relevant provisions

Article 7 and Annex I, Section 7 – Grand Challenges

Rationale

The proposal recognises advanced materials in relation to pilot lines and specialty semiconductor technologies. Annex I already refers to architectures and materials for power electronics, neuromorphic and embedded AI chips, integrated photonics, graphene and other two-dimensional-material technologies. Nevertheless, the role of advanced materials could be expressed more prominently in the Grand Challenges framework. Europe's future competitiveness in AI hardware, neuromorphic computing, photonics, sensing, power electronics and quantum technologies will depend not only on conventional semiconductor scaling, but also on identifying, processing and integrating new functional materials.

A dedicated emphasis on advanced materials would diversify Europe's semiconductor research and innovation portfolio and reduce the risk of concentrating investments exclusively on established technology roadmaps.

A complementary need is sustained research on new semiconductor manufacturing processes. Europe's earlier strength in areas such as lithography, plasma-based etching and deposition, surface modification, integration and packaging was supported by research groups working upstream of industrial deployment. A balanced portfolio of low- and medium-TRL activities is needed to regenerate this knowledge base, develop new processes alongside new equipment and materials, and train specialists able to transfer these capabilities to industry.

Proposed addition to Article 7

The Grand Challenges may also support the discovery, development, integration and industrial validation of advanced functional materials and new manufacturing processes for next-generation semiconductor, photonic, neuromorphic, quantum and AI hardware technologies. This should include front-end and back-end processing, manufacturing equipment and process development, with an appropriate mix of low- and medium-TRL research to generate new knowledge, strengthen European R&D capabilities and develop specialised talent.

Proposed addition to Annex I, Section 7

A Grand Challenge may address advanced materials for future computing and sensing systems. Such a challenge should support the identification, processing, integration and validation of materials capable of enabling substantial improvements in computing performance, energy efficiency, sensing capability, security and functionality. Particular attention should be given to their compatibility with existing semiconductor manufacturing processes and their potential industrial scalability.

2. AI as an enabler of semiconductor manufacturing, materials optimisation and metrology

Relevant provisions

Article 7 and Annex I, Section 7 – Grand Challenges

Rationale

The proposal strongly emphasises the role of advanced semiconductors and AI chips in enabling the development and deployment of increasingly powerful AI models. NCSR Demokritos considers that the complementary direction of this relationship should also be explicitly recognised: AI can serve as a major enabling technology for improving semiconductor manufacturing itself. This two-way relationship can create a positive feedback loop in which advances in semiconductor technologies support more capable AI systems, while advances in AI accelerate the discovery, optimisation, fabrication and quality control of semiconductor materials and devices.

AI-driven methods are already being applied across different stages of semiconductor development, but relevant European activities remain fragmented. Applications include computational materials discovery and resist design; optimisation of lithography, etching, deposition and atomic layer deposition processes; predictive process control and equipment maintenance; defect detection and classification; image reconstruction and noise reduction; and high-precision metrological characterisation of fabricated structures. Better coordination at Union level would accelerate methodological development, promote access to high-quality and interoperable datasets, and enable a realistic, independently validated assessment of the contribution of AI at different stages of semiconductor design and manufacturing.

Proposed addition to Article 7 and Annex I, Section 7

A Grand Challenge may support the coordination, development and industrial validation of AI-driven methods for semiconductor manufacturing, focusing on: (a) the discovery and optimisation of materials; (b) the optimisation, monitoring and control of manufacturing processes; and (c) the metrological characterisation, inspection and defect analysis of semiconductor structures, including patterns requiring sub-nanometre accuracy. Actions should promote interoperable and high-quality datasets, physics-informed and trustworthy AI models, common benchmarking and validation protocols, and demonstration in pilot-line and industrial

environments. Particular attention should be given to quantifying improvements in process efficiency, yield, reproducibility, resource and energy use, and measurement accuracy.

3. Flexible pilot lines for advanced materials and specialty technologies

Relevant provisions

Article 5 and Annex I, Section 2 – Pilot lines for preparing for innovative production, testing and validation

Rationale

The proposal provides for new or upgraded pilot lines addressing emerging technological challenges. This is strongly welcomed. However, the implementation framework should also accommodate flexible and distributed pilot-line models that can evaluate emerging materials and processes before they are sufficiently mature to justify investment in a large, fully integrated pilot line. Europe has substantial specialist capabilities distributed among RTOs, universities, cleanrooms and regional facilities. These capabilities can contribute to the intermediate innovation stage between laboratory research and large-scale pilot-line validation, particularly around TRL 4–6. Their role should be explicitly recognised and connected to the larger European pilot-line ecosystem.

Proposed addition

New or upgraded pilot lines and pilot testbeds may include flexible or distributed infrastructures dedicated to the evaluation of advanced materials, specialty semiconductor platforms and emerging fabrication processes. Such infrastructures should support:

- the assessment of compatibility with semiconductor manufacturing processes;
- process integration and repeatability studies;
- the development of process design kits and validated process modules;
- in-line and end-of-line metrology, inspection and quality control;
- device fabrication, characterisation and reliability assessment; and
- the transfer of validated processes to larger pilot lines or industrial manufacturing facilities.

The implementation framework should also provide transparent criteria through which existing cleanrooms and research infrastructures may progress towards recognition as pilot testbeds or pilot lines.

4. Convergence of AI, semiconductor and quantum technologies

Relevant provisions

Article 5 and Annex I, Sections 1, 3 and 7

Rationale

The proposal separately addresses AI-oriented semiconductor technologies and quantum chips. However, increasing convergence is expected between quantum processing, conventional semiconductor control electronics, photonic technologies, advanced packaging, AI accelerators and AI-enabled control and optimisation. Future European programmes should therefore support integrated hardware architectures rather than treating AI and quantum technologies exclusively as separate technological domains.

Proposed addition

The Chips for Europe Initiative 2.0 shall support research, design, prototyping and industrialisation activities addressing the convergence of AI chips, conventional semiconductor technologies, photonic technologies and quantum chips. This may include integrated architectures for quantum control and readout, AI-assisted quantum systems, heterogeneous integration, advanced packaging and the development of common design, testing and validation methodologies. This convergence should also be reflected in relevant Grand Challenges, Design Platform capabilities and future pilot-line work programmes.

5. Upgrading the facilities of Competence Centres

Relevant provisions

Article 4(d), Article 5(d), Article 6(4) and Annex I, Section 4

Rationale

Operational Objective 4 refers to supporting a network of competence centres by enhancing existing facilities or creating new facilities. However, this intention is not equally explicit in the actions listed under Article 5. Competence Centres cannot provide state-of-the-art services exclusively through coordination, advisory support and training. Their ability to support SMEs, start-ups, scale-ups, researchers and end users also depends on access to up-to-date technical infrastructure, specialised equipment and testing and validation capacities. The possibility of upgrading existing facilities or creating new facilities should therefore be expressly included among the eligible actions of the Initiative.

Proposed replacement of Article 5(d)(i)

(i) strengthen the capacities of competence centres, including through the upgrading of existing facilities or the creation of new facilities, and enable them to offer a wide range of expertise and state-of-the-art services to stakeholders, including end-user start-ups, scale-ups and SMEs, while facilitating access to, and the effective use of, the capacities and facilities referred to in this Article;

Proposed amendment to Article 6(4)

4. The competence centres shall have substantial overall autonomy to determine their organisation, composition and working methods. Their organisation, composition, facility-development and upgrading plans, and working methods shall comply with and contribute to the objectives of this Regulation and the Chips for Europe Initiative 2.0.

Additional implementation recommendation

Future support for Competence Centres should distinguish between:

1. operational funding for coordination, training and service delivery;
2. access to shared European infrastructures;
3. investment funding for equipment renewal and facility upgrading; and
4. support for the creation of new specialised capacities where justified by technological and market needs.

Without a mechanism for continuous technological renewal, Competence Centres may progressively lose the capacity to offer services that correspond to the evolving needs of European industry.

6. Expanded role and performance framework for Competence Centres

Relevant provisions

Article 6 and Annex I, Section 4

Rationale

Training and skills development constitute an essential component of the Competence Centres' mission. Nevertheless, their contribution should not be evaluated mainly through the number of training activities or participants. Competence Centres should function as active gateways connecting SMEs, start-ups, scale-ups, researchers and end-user industries with the Design Platform, pilot lines, Grand Challenges, Strategic Projects, investment instruments and specialised expertise available across Europe.

Proposed addition

The performance framework for competence centres should include indicators covering:

- support provided to SMEs, start-ups, scale-ups and end-user industries;

- referrals and successful access to pilot lines and the Design Platform;
- technology-transfer and innovation-support activities;
- prototypes, demonstrators and validated designs supported;
- cross-border services and collaborations;
- industrial engagement and private investment mobilised;
- contributions to Strategic Projects and Grand Challenges;
- specialised training, upskilling and reskilling activities; and
- the development or upgrading of technical facilities and services.

The continuation, refocusing or creation of Competence Centres should be based on demonstrated performance, technological specialisation, market demand and regional and European ecosystem needs.

7. Transparent access to pilot lines, PDKs and Design Platform services

Relevant provisions

Article 5 and Annex I, Sections 1 and 2

Rationale

Open access to pilot lines, Process Design Kits and Design Platform services is one of the most important features of the proposed framework. As demand increases, access allocation could become a significant barrier for RTOs, universities, SMEs and start-ups. Preferential treatment for Strategic Projects should not result in open access being limited to residual capacity.

Proposed implementation provisions

The Commission and the Chips Joint Undertaking should establish harmonised and auditable principles covering:

- eligibility and technical-readiness requirements;
- access-allocation criteria when demand exceeds capacity;
- transparent and appropriately priced access;
- indicative access windows or capacity for SMEs, RTOs, universities and non-Strategic-Project users;
- justification of rejected access requests;
- review or appeal procedures;
- management of confidential information and intellectual property; and
- coordination between competence centres, the Design Platform and pilot-line operators.

Consortia operating publicly supported infrastructures should report periodically on the distribution of access among Strategic Projects, SMEs, start-ups, universities, RTOs and other user categories.

8. Governance and openness of Grand Challenges

Relevant provisions

Article 7 and Annex I, Section 7

Rationale

Grand Challenges can overcome fragmentation and mobilise European capabilities around strategic missions. However, their success will depend on transparent selection, measurable objectives and the ability to incorporate emerging technologies and newly identified capabilities.

Grand Challenges should not become closed structures determined solely by the organisations involved at their creation.

Proposed addition

The implementation framework should specify:

- how Grand Challenges are identified and selected;
- the evidence, foresight and consultation processes supporting their selection;
- measurable objectives, milestones and success indicators;
- independent monitoring and technical review;

- procedures for restructuring, re-scoping or terminating underperforming initiatives;
- mechanisms through which new partners and capabilities may join an ongoing Grand Challenge;
  - conflict-of-interest safeguards; and
  - limits or safeguards concerning excessive concentration of available funding.
  - dedicated low- and medium-TRL research tracks for new front-end and back-end processing, manufacturing equipment and advanced materials, including emerging process technologies with potential future semiconductor relevance.

Consortia proposing Grand Challenges should be required to demonstrate that they have mapped relevant technological capabilities across the Union and explain how these capabilities have been incorporated, connected to the mission or considered unnecessary. This capability-based approach would promote meaningful participation without creating automatic institutional or geographical quotas.

9. Recognition and governance of European Semiconductor Technology Initiatives

Relevant provisions

Articles 13–15

Rationale

Recognition as a European Semiconductor Technology Initiative should be based on European strategic value, technical excellence, cross-border impact and contribution to security of supply. The process should remain consistent across the Union and should not be exposed to fragmented national procedures or diverging national interests. At the same time, Member States have legitimate roles regarding permitting, national co-financing and regional implementation. Their involvement should therefore not be entirely excluded, but the recognition, evaluation and monitoring framework should remain European and centrally coordinated.

Proposed addition to Article 15

The granting, periodic review, monitoring and, where applicable, withdrawal of the status of a European Semiconductor Technology Initiative shall be conducted through a transparent and harmonised Union-level procedure led by the Commission, supported by independent technical expertise and consultation with the European Semiconductor Board. The evaluation shall assess technological excellence, contribution to Union strategic objectives, cross-border impact, security of supply, accessibility, implementation capacity, financial sustainability and compliance with the requirements of this Regulation. Relevant Union programmes and instruments may be used to organise independent technical evaluation and monitoring.

In parallel, open research actions at low and medium TRL should support the exploration and integration of emerging and adjacent manufacturing technologies that may strengthen future semiconductor capabilities. These may include surface-engineering technologies (including plasma surface engineering), additive and 3D manufacturing approaches relevant to packaging and integration, and new technologies for reducing or treating chemicals and other manufacturing waste. Successful outcomes should be eligible for further evaluation and, where they demonstrate sufficient strategic and technological relevance, progression towards European Semiconductor Technology Initiative activities.

10. Dedicated support for the upscaling of advanced-material devices and circuits

Relevant provisions

Article 17 and Annex II

Rationale

Annex II concentrates on a limited set of large strategic areas. A further priority could address the industrial upscaling of devices and circuits based on advanced materials that are compatible with semiconductor processing. This would create an industrialisation pathway for technologies developed within European research organisations and specialised pilot facilities but not yet represented within dominant manufacturing roadmaps.

Proposed additional priority area in Annex II

Upscaling of advanced-material semiconductor devices and circuits

This priority area shall support the transition of advanced-material devices and circuits from laboratory validation to pilot-scale and industrially relevant manufacturing. Activities may include:

- material synthesis and wafer-level processing;
- compatibility with CMOS and other established semiconductor processes;
- device and circuit fabrication;
- heterogeneous integration and advanced packaging;
- process control, metrology and inspection;
- reliability, qualification and standardisation;
- development of Process Design Kits;
- demonstration in strategically relevant applications; and
- transfer to European pilot lines and manufacturing facilities.

Potential applications may include AI and neuromorphic computing, quantum technologies, photonics, sensing, power electronics, healthcare, communications, space, security and defence.

11. Financial support for Strategic Projects

Relevant provisions

Articles 16, 18 and 20

Rationale

Article 16 defines the conditions for recognition as a Strategic Project, while Article 20 enables the Commission to coordinate and crowd in investments. Recognition and financing, however, should remain legally distinct: recognition as a Strategic Project cannot automatically guarantee a grant. Nevertheless, Strategic Projects will often require substantial public support because of their scale, technological risk, cross-border nature and strategic importance. The Regulation should therefore include a clearer commitment to facilitate access to appropriate Union and national financing instruments.

Proposed addition to Article 18 or Article 20

Strategic Projects shall be eligible to receive financial support through relevant Union and national programmes and financial instruments, subject to the applicable selection procedures, budget availability, State-aid rules and other requirements of Union law. The Commission, in cooperation with the Chips Joint Undertaking, Member States, the European Investment Bank and other relevant financial institutions, should facilitate the preparation of coordinated financing packages combining grants, equity, guarantees, loans and national co-financing where appropriate. This formulation provides meaningful financial support without creating an unconditional entitlement to a grant merely through designation as a Strategic Project.

12. Circularity, recycling and reuse of semiconductor components

Relevant provisions

Article 17 and Annex II

Rationale

Annex I already recognises that Grand Challenges may address recycling and increased circularity of materials. Nevertheless, circularity should also be reflected in the priority areas for Strategic Projects, given the strategic importance of critical raw materials, the environmental footprint of semiconductor manufacturing and the increasing volume of electronic waste. The scope should extend beyond recycling to include component reuse, remanufacturing, testing, traceability and recovery of critical materials.

Proposed additional priority area in Annex II

Circular semiconductor technologies and reuse of electronic components

Strategic Projects may support the development and industrial deployment of technologies and value chains for:

- recovery and recycling of semiconductor materials and critical raw materials;
- safe extraction, testing and qualification of reusable electronic and semiconductor components;
- remanufacturing and life extension of electronic systems;
- traceability and digital product information supporting component reuse;
- design-for-disassembly, repair, reuse and recycling;
- reduction and recycling of water and chemicals used in semiconductor manufacturing;
- waste-heat recovery and energy-efficient manufacturing; and
- industrial-scale demonstration of circular semiconductor production models.

Activities should take account of reliability, safety, cybersecurity, intellectual-property protection and the requirements of critical applications.

13. Technical working groups supporting the European Semiconductor Board

Relevant provision

Article 44

Rationale

The proposal allows the European Semiconductor Board to establish subgroups and involve experts. This possibility should be transformed into a more systematic mechanism for obtaining scientific and technical advice. The Board will be required to provide opinions on priority areas, Strategic Projects, Grand Challenges, infrastructure development and supply-chain resilience. These decisions require continuous technical input from organisations that design technologies and operate European research and pilot infrastructures.

Proposed addition to Article 44

The European Semiconductor Board may establish standing or time-limited technical working groups and horizontal task forces to support the preparation of technology roadmaps, vision papers, concept notes, recommendations and opinions. Technical working groups may address the priority areas identified in Annex II and other emerging technological domains. They should include balanced representation from Research and Technology Organisations, universities, industry, SMEs, pilot-line operators, competence centres, Strategic Projects and relevant end-user sectors.

Horizontal task forces may address cross-cutting matters such as skills, sustainability, circularity, metrology, research security, access to infrastructure, intellectual property, industrialisation pathways and supply-chain resilience. Members shall be selected through transparent procedures on the basis of relevant expertise and shall be subject to appropriate conflict-of-interest and confidentiality requirements. Representatives of Strategic Projects and European Semiconductor Technology Initiatives may participate, but the groups should not be composed exclusively of representatives of the initiatives being assessed. Independent scientific and technical expertise must also be included.

14. Continuity between research, pilot validation and industrial deployment

Relevant provisions

Articles 5, 7, 18 and 20

Rationale

The proposal combines Horizon Europe, the Chips for Europe Initiative, Digital Europe, InvestEU and other instruments. However, promising technologies may still encounter a financing and implementation gap between research validation and access to larger pilot or industrial facilities. This intermediate stage is particularly important for RTOs and specialised research infrastructures that mature technologies approximately from TRL 4 to TRL 6.

Proposed implementation recommendation

The Commission should establish a structured "lab-to-pilot-to-fab" pathway comprising:

- technical maturity assessment;
- preparation for access to pilot lines;
- small-scale validation and process-development support;
- grants or vouchers covering access and adaptation costs;
- support for PDK development and process qualification;
- industrial mentoring and identification of potential adopters;
- follow-on financing for successful results; and
- monitoring of progression between programmes and Technology Readiness Levels.

Competence Centres could serve as entry points and case managers for these pathways, while responsibility for coordination and follow-up should be clearly assigned at European level.

15. Long-term sustainability and technological renewal of pilot lines

Relevant provisions

Article 5 and Annex I, Section 2

Rationale

Pilot lines require continuous investment in maintenance, operation, staff, equipment renewal and technological upgrading. Utilisation rates alone do not adequately measure their contribution to European industrialisation.

Proposed implementation recommendation

The long-term performance framework for pilot lines should include:

- external users and cross-border users served;
- validated processes and Process Design Kits;
- external tape-outs and prototypes;
- technologies transferred to industry;
- processes qualified by industrial users;
- patents, licences and spin-offs;
- follow-on private investment;
- progression towards commercial manufacturing;
- contribution to Strategic Projects and Grand Challenges; and
- energy, water, materials and circularity performance.

Future decisions regarding the creation, expansion, refocusing or discontinuation of pilot lines should follow a transparent European procedure based on technological developments, industrial demand, strategic dependencies and demonstrated performance.

16. Active participation of RTOs in the Industrial Alliance for Semiconductors

Rationale

The Industrial Alliance for Semiconductors can become an important mechanism connecting European policy, research capacities, manufacturing capabilities and demand from end-user industries.Its membership and governance should therefore ensure effective participation by Research and Technology Organisations and public research infrastructures, alongside semiconductor manufacturers, equipment providers, materials suppliers, design companies and end users.

Proposed recommendation

The governance and activities of the Industrial Alliance for Semiconductors should ensure balanced representation across the semiconductor value chain, including Research and Technology Organisations, universities, Competence Centres, pilot-line operators, SMEs, start-ups, scale-ups, large industrial companies and end-user sectors. The Alliance should systematically map existing European research, cleanroom, fabrication, characterisation, testing and packaging capabilities and use this mapping when preparing technology roadmaps, investment priorities and demand-acceleration activities. Research organisations should participate not only as training providers, but as technology-development, prototyping, fabrication, characterisation and industrialisation partners.

17. Simplification of administration for co-financed semiconductor projects

Relevant provision

Article 24 – Use of European Business Wallets and administrative simplification

Rationale

Chips Joint Undertaking actions that rely on substantial national co-financing can create unnecessary administrative duplication when beneficiaries must pass through separate European and national calls, evaluations, reporting systems and financial controls for the same project. This duplication increases delays and administrative workload for public authorities and beneficiaries, reduces productivity and is difficult to reconcile with the speed required in a fast-moving technological field.

Proposed addition to Article 24

For projects co-financed at Union and Member-State level, the implementation framework should remove duplication from proposal submission through project implementation and closure. To the greatest extent possible, co-financed actions should operate through one coordinated call and evaluation, a single or fully aligned contractual framework, one technical reporting system and one set of financial reporting and audit requirements. European Business Wallets and interoperable national portals should be used to enable the once-only submission and reuse of administrative information across Union and national authorities.